REMARKS

In accordance with the foregoing, claims 2-6 are pending. Claim 1 has been canceled without prejudice or disclaimer. Claim 2 has been amended into independent form. The specification has been amended and the drawings have been amended in the attached Request for Approval of Drawing Corrections. No new matter is presented.

The drawings were objected to due to various informalities. The drawings have been amended in accordance with the attached Request for Approval of Drawing Corrections to label Figs. 19 and 21 as prior art. Regarding the reference elements which were excluded from Fig. 19, the specification has been amended to delete these reference elements. These reference elements are unnecessary for one of ordinary skill in the art to understand the claimed invention. Accordingly, Applicant requests that this objection be withdrawn.

Claims 1-2 were rejected under 35 USC 102(e) as being anticipated by Tanaka (U.S. Patent No. 6,285,591). This rejection is respectfully traversed.

The rejection of claim 1 is moot in view of the foregoing amendments.

Claim 2 recites that "the negative second voltage has an absolute value smaller than an absolute value of the negative first voltage." Thus, the absolute value of the voltage applied to the non-select row lines is smaller than the absolute voltage applied to the substrate or well. Tanaka does not disclose or suggest this feature.

Tanaka discloses a negative voltage, such as -12V, being applied to a P-well type region and a negative voltage, such as -12V, being applied to the non-selected word lines (see col. 18, lines 28-39). The absolute value of these voltages are equal. Tanaka fails to disclose or suggest that the absolute value of the voltage applied to the non-select row lines is smaller than the

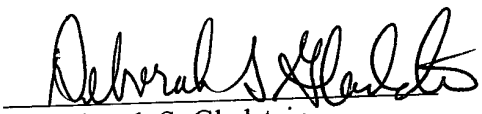
absolute voltage applied to the substrate or well. Accordingly, the features of claim 2 are neither disclosed nor suggested by Tanaka. Applicant requests that this rejection be withdrawn.

Attached hereto is a marked-up version of the changes made by this amendment, captioned "**Version with markings to show changes made**".

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing 204552018400.

Dated: August 23, 2002

Respectfully submitted,

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Amend the paragraph from page 3, line 20 through page 4, line 8, as follows:

The ACT type flash memory is so constructed that a control gate 1, an interlayer insulator 2, a floating gate 3 and a tunnel oxide 4 are formed in layers so as to stretch over a drain 6 and a source 7 provided in a substrate (P-type well) 5. It is noted that the drain 6 and the source 7 have different donor concentrations. Then, in the program operation in which electrons are pulled out from the floating gate 3, a negative voltage [Vnw (] of -8 V[)] is applied to the control gate 1 and a positive voltage [Vpp (] of +5 V[)] is applied to the drain 6 so that the source 7 is put into a floating state, where the electrons are pulled out from the floating gate 3 by the FN tunneling phenomenon. As a result, the threshold of the memory cell to be programmed is lowered to about 1.5 V.

Amend the paragraph beginning on page 4, line 9, as follows:

Also, in the erase operation in which electrons are injected into the floating gate 3, a positive voltage [Vpe (] of +10 V[)] is applied to the control gate 1, a negative voltage [Vns (] of -8 V[)] is applied to the source 7 and a negative voltage of -8 V is applied to the drain 6, where the electrons are injected into the floating gate 3 by the FN tunneling phenomenon. As a result, the threshold of the cell to be erased is increased so as to rise to about 4 V or more. Like this, the ACT type flash memory is an FN-FN type flash memory.

IN THE CLAIMS:

Claim 1 has been cancelled without prejudice.

Amend claim 2 as follows:

2. (Amended) [The] An erase method for a nonvolatile semiconductor storage device [according to claim 1] in which floating gate field effect transistors each having a control gate, a floating gate, a drain and a source and being electrically information programmable and erasable are arrayed in a matrix shape on a substrate or well, and which comprises a plurality of row lines connected to the control gate of each floating gate field effect transistors arrayed along a row direction, and a plurality of column lines connected to the drain and source of each floating gate field effect transistors arrayed along a column direction, the method comprising:

using the Fowler-Nordheim tunneling phenomenon for both programming and erasing; and

for erasing, applying a negative first voltage to the substrate or well and applying a positive voltage to select row lines, while applying a negative second voltage to non-select row lines, wherein

the negative second voltage has an absolute value not larger than an absolute value of the negative first voltage.